AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) An arrangement for capturing data from a data stream of a predetermined data transfer rate, comprising:

a first flip-flop that is adapted to receive the data stream on its data input and a system clock signal on its clock input for clocking captured data to its output,

a symmetrical multiphase clock generator that is adapted to be locked to a reference clock which in turn is adapted to generate a reference clock signal at the data transfer rate or at a fraction thereof, the multiphase clock generator being adapted to generate n clock signals mutually shifted in phase 360°/n from each other, where n is an integer, and

a selector that is connected with its input to the multiphase clock generator to receive the n clock signals, the selector being adapted to select, in response to a control signal, one of these n clock signals to be the system clock signal to be supplied to the clock input of the first flip-flop, wherein

a dual edge triggered second flip-flop is connected with its data input to the clock input of the first flip-flop and with its clock input to the data input of the first flip-flop to sample the selected system clock signal by means of the incoming data stream on every data transition thereof to generate on its output a retard clock signal that is high if the selected system clock signal is high when sampled and that is low if the selected system clock signal is low when sampled,

a divider is connected with its input to the data input of the first flip-flop and is adapted to generate a counter clock signal on its output every time a predetermined number of data transitions has occurred in the data stream, and

a clock phase counter is connected with its input to the output of the dual edge triggered second flip-flop, with its clock input to the output of the divider, and with its output to the selector to control the selector to select another one of said n clock signals to be the system clock signal in response to the retard clock signal being high or low.

2. (Original) The arrangement according to claim 1, **characterized in** that said predetermined number is ≥ 2.